Remarks

Reconsideration of this application as amended for prosecution is respectfully requested.

The Examiner rejected claims 1-14, 19-21, and 25-29. Claims 1-3, 5-7, and 11-14 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,088,264 of Hazen ("Hazen"). Claims 19-21 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,201,739 of Brown ("Brown"). Claims 8-10 and 25-28 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,822,244 of Hansen ("Hansen"). Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Hazen in view of U.S. Patent 6,377,486 of Lee ("Lee").

The Examiner objected to Claim 8 for informalities. Claim 8 has been amended to correct the informalities.

Applicants submit that claim 1 as amended is not anticipated under 35 U.S.C. § 102(e) by Hazen. Claim 1 includes the limitations:

> dividing the memory device into k partitions, wherein k is an integer greater than or equal to two;
> performing code operations from m code partitions out of k total partitions, wherein m is an integer greater than or equal to one;
> performing data operations from n data partitions out of k total partitions through low level functions accessed from the code partitions at approximately the same time as the code operations are performed from the m code partitions, wherein n is an integer greater than or equal to one; and
> <u>suspending the data operations of the n data partitions if a preempting operation is detected.</u>

(Amended claim 1) (emphasis added).

In contrast, Hazen discloses a flash memory partitioning for read-while-write operation that permits simultaneous access to more than one subsection of the flash memory. (Hazen, column 2, lines 23-38). Hazen further discloses an example of a three partitioned flash memory device that has code executed from a first partition, while updating data in a second partition. (Hazen, column 3, lines 55-59). Hazen, however, does not disclose suspending the data operations of the n data partitions if a preempting operation is detected.

Moreover, Hazen does not disclose performing data operations from n data partitions out of k total partitions through low level functions accessed from the code partitions.

Given that claims 2-7 depend from claim 1, applicants submit that claims 2-7 are not anticipated under § 102(e) or rendered obvious under § 103(a) by the references cited by the Examiner.

Applicants submit that claim 8 as amended is not anticipated under 35 U.S.C. § 102(b) by Hansen. Claim 8 includes the limitations:

> means for partitioning a memory device into a first plurality of partitions for storing code and a second plurality of partitions for storing data to enable multiple operations to be performed on a memory device at the same time; and
> means for setting each of the partitions to a status mode to track operations performed on the memory device.

(Claim 8) (emphasis added).

In contrast, Hansen discloses a flash memory 12 that includes memory arrays 20 and 22 and control and registers 24. (Hanson, column 3, lines 35-36). Hanson does not disclose a means for partitioning a memory device into a first

plurality of partitions for storing code and a second plurality of partitions for storing data as set forth in amended claim 8. Moreover, even if Hanson did disclose a means for partitioning a memory device into a first plurality of partitions for storing code and a second plurality of partitions for storing data, Hanson fails to disclose a means for setting each of the partitions to a status mode to track operations performed on the memory device.

Given that claims 9-10 depend from claim 8, applicants submit that claims 9-10 are not anticipated under § 102(b) by the reference cited by the Examiner.

Applicants submit that claim 11 as amended is not anticipated under 35 U.S.C. § 102(e) by Hazen. Claim 11 includes the limitations:

> a data partition;
> a code partition;
> a status mode to provide a partition status from the memory array if a task request is received by the data partition, wherein if the partition status is busy, an algorithm in the code partition determines whether the task request preempts an existing task;
> a read mode to enable code and data to be read from the memory array; and
> a write mode to enable data to be written to the memory array.

(Claim 11) (emphasis added).

In contrast, Hazen discloses a multi-partitioned flash memory device... Each partition has associated an X decoder and a Y selector... Having multiple X selectors and Y decoders permits simultaneous access to more than one subsection of the flash memory. For example, while partition A may be erased, partition B may simultaneously be read... A memory in partition A may be written to, while a memory block in partition B is erased. (Hazen, column 2, lines

25-42). Thus, Hazen only discloses the write operation and read operation itself. Hazen fails to disclose a memory array having a read mode to **enable** a read operation and a write mode to **enable** a write operation.

Further, even if Hazen did disclose a read mode to enable code and data to be read from the memory device and a write mode to enable data to be written to the memory device, Hazen does not disclose a status mode to provide a partition status from the memory array if a task request if received by the data partition, wherein if the data partition is busy, an algorithm in the code partition determines whether the task request preempts an existing task.

Given that claims 12-14 depend from claim 11, applicants submit that claims 12-14 are not anticipated under § 102(e) by the reference cited by the Examiner.

Applicants submit that claim 19 as amended is not anticipated under 35 U.S.C. § 102(e) by Brown. Claim 19 includes the limitations:

> a memory device having a code partition and a data partition, wherein the code partition comprises a low level function that is performed on data stored in the data partition; and
> a flag to indicate when a suspend operation has occurred.

(Claim 19) (emphasis added).

In contrast, Brown discloses a flash EPROM that stores both code and data. (Brown, column 9, line 49). Brown does not disclose a memory device having a code partition and a data partition, wherein the code partition comprises a low level function that is performed on data stored in the data partition.

Given that claims 20-21 depend from claim 19, applicants submit that

claims 20-21 are not anticipated under § 102(e) by the reference cited by the Examiner.

Applicants submit that claim 25 as amended is not anticipated under 35 U.S.C. § 102(b) by Hansen. Claim 25 includes the limitations:

> running a first operation of a first partition of a memory array;
> running a first operation of a second partition of the memory array;
> requesting a second operation to be performed on the second partition; and
> determining from the first operation of the first partition if the second operation of the second partition has a higher priority than the first operation of the second partition.

(Claim 25) (emphasis added).

In contrast, Figure 4 of Hansen discloses a flow diagram of a suspend operation of flash memory 12. At a decision step 44, it is determined if a program or erase operation is currently active in the blank being accessed. If a program or erase operation is currently active... the program or erase operation is suspended, as shown in step 48, for a read operation to occur. (Hansen, column 5, lines 10-16). Hansen, however, does not disclose determining from the operation of another partition whether to suspend the program or erase operation for the read partition.

Given that claims 26-29 depend from claim 25, applicants submit that claims 26-29 are not anticipated under § 102(e) by the reference cited by the Examiner.

Respectfully submitted,

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